IN THE SPECIFICATION:

Please rewrite the paragraph at page 2, lines 10-25, so that it reads as follows:

However, if the I/O pad 20 receives a 5V input logic signal, it subjects the PMOS transistor P1 to a gate voltage of 3.3V, a drain voltage of 5V, and a source voltage of 3.3V. Since the gate voltage (3.3 V) is lower than the drain voltage (5 V) at the PMOS transistor P1, the gate voltage switches the PMOS transistor P1 to a reverse conducting state. Moreover, since the PMOS transistor P1 is formed on an N-type substrate and its source and drain are both P-type, a PN junction diode is formed between its drain and the N-well. Furthermore, since the drain of the PMOS transistor P1 is connected to the I/O pad 20, now receiving the 5 V input logic signal, higher than the 3.3V system voltage, and the substrate thereof is connected to the 3.3V system voltage, the PN junction diode is subjected to a forward bias, causing an undesired large current to flow between the external 5V source and the internal 3.3V source.

Please rewrite the paragraph at page 2, line 26 through page 3, line 9, so that it reads as follows:

As a solution, an improved I/O buffer for the 3.3V IC is disclosed. FIG. 2 is a schematic diagram showing an I/O buffer capable of accepting an input logic signal voltage higher than the system voltage. The P-gate control circuit 32 conveys the first gate control signal Vp to the PMOS transistor Q3 of the I/O circuit. The N-well control circuit 34 adjusts the voltage at the floating N-well of the PMOS transistor Q3 according to the input voltage at the I/O pad 36. Undesired current leakage is thus prevented. In this I/O buffer, however, transistors Q5 and Q6 are required to follow design ~~rule~~ rules

for electrostatic discharge (ESD) protection because the transistors Q5 and Q6 of the P-gate control circuit 32 are connected to the I/O pad 36 directly. Thus, it occupies a larger wafer area.